正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AC5035

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Customer APPROVED	
Company	
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PREPARED	REVIEW			APPROVED	DCC ISSUE
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正基科技股份有限公司

AC5035

Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2024/06/26	Preliminary Release	Ike
0.2	2024/07/04	HW and SW review	Ike
0.3	2024/07/19	Update function temperature spec.	Ike
0.4	2025/03/14	Update 2D dimension layout picture	Nixon
0.5	2025/04/23	Modify UIM name to UIM0 & UIM1	Nixon
0.6	2026/09/09	Modify Table 5-2 Sub-6 5G NR	Nixon

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1. Introduction

1.1 Overview

The AMPAK Technology® AC5035 module is a multipurpose 3GPP Release 17 Redcap module. It was envisioned to operate in conjunction with a host board that must provide power and control for its various applications. The module chipset is Qualcomm SDX35, which supports 4G and 5G technologies and was designed with an advanced 4 nm process for superior performance and power efficiency.

1.2 Block Diagram

The following figure presents the high-level block diagram of the SDX35 global LGA module, including the baseband (BB) and radio frequency (RF) chipset along with its most important interfaces and connectors. The illustration provides a visual representation of the module and helps understand its framework.

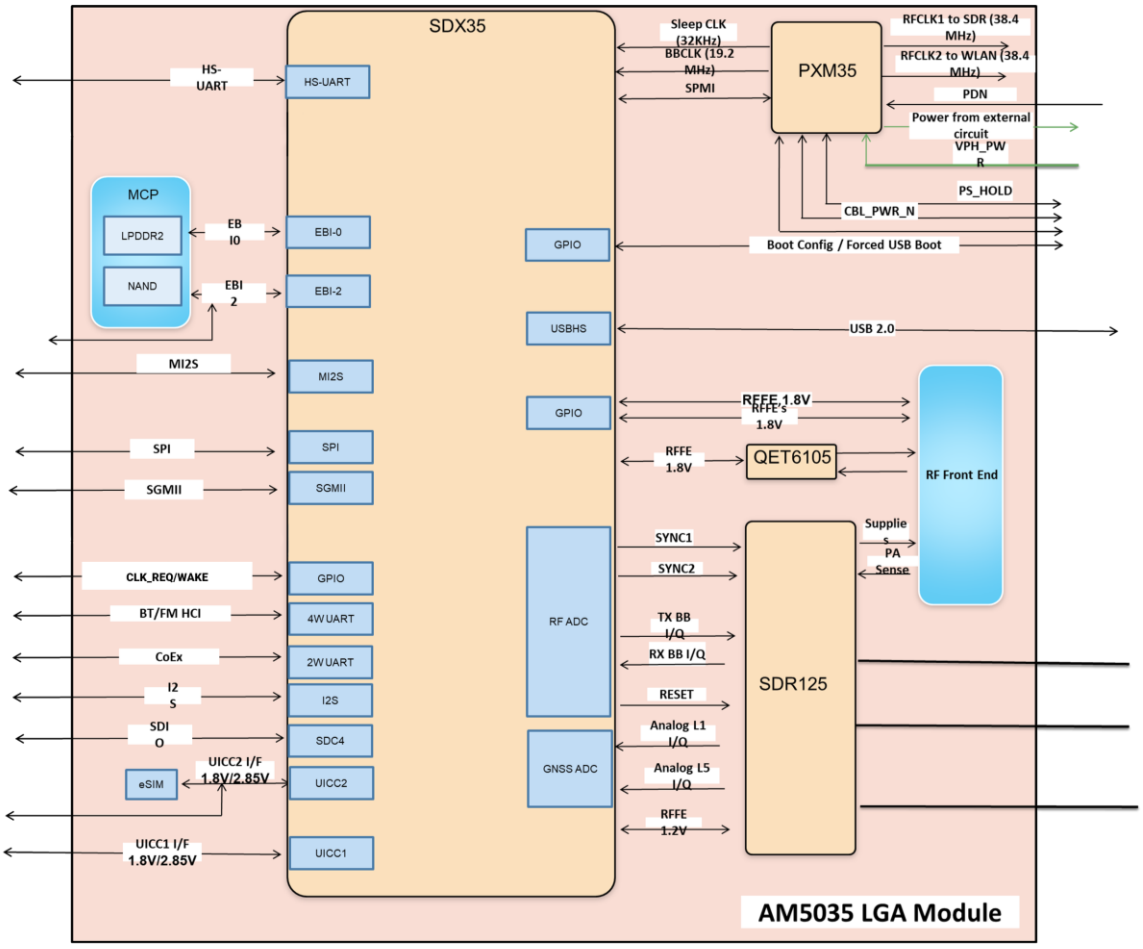

Figure 1-1 Global LGA module High-level block diagram

2. General Specification

2.1 Features

Table 2-1 Module features

Feature	Description
Processors	
Applications	Arm Cortex A7 processor up to 1.7 GHz
Modem system	Qualcomm® Hexagon™ DSP processor up to 1364 MHz (Turbo)
Always-on subsystem	Cortex-M3 up to 400 MHz Hardware-based resource and power management
Memory and storage support	
Memory	LP2 533 MHz
Connectivity	
QUP ports UART I^2C SPI (master only)	Four, 4 bits each; multiplexed serial interface functions Yes: four instances (each 4-bit wide) up to 4 MHz Yes Yes; up to 50 MHz
UIM	UIM1 UIM2 (internally connected to an eSIM (optional) card but can be used externally as well)
USB	One HS USB 2.0
Audio Interfaces	Primary and secondary I^2S and PCM
Ethernet	One SGMII
RF support	
Standard compliance	3GPP Release 17 5G RedCap
Multimode support	5G NR Sub-6 (FR1) SA and 4G LTE CAT4
Supported bands	See Table 5-2
Antenna ports	2x WWAN + 1 GNSS
Technology frequency range	FR1 (4G, 5G-NR): 0.6 GHz to 5.0 GHz
Maximum bandwidth	20 MHz, No CA

Modulation	UL-256QAM; DL-256QAM
WLAN/WAN concurrency	WL to N79 N79 to WL
DL MIMO	2 × 2 Rx: All 4G and 5G LMHB and UHF bands,
Tx power class (HPUE)	PC2: BN40, BN41, B42, N77, N78, N79
SRS	1T/2R(TDD_LTE, TDD_NR SA)
Antenna switch diversity (ASDIV)	Yes
GNSS	GPS, GLONASS, Galileo, and BeiDou support下面紅色Mark 刪除 Two GNSS paths to support simultaneous L1 and L2/L5
Additional support	
Clock outputs	RF clock: 38.4 MHz Sleep clock: 32.7645 kHz
Debug	UART
Display	EBI2
Key module chips	
Modem	SDX35
Memory and storage	JSFCBA3YH3BBG-425A MCP
eSIM(optional)	MFXS-M006b-MFOCMW
Transceiver	SDR125
RF front end	QPA6590, QPM6579, QDM5302, QFM6515
Envelop tracker	QET6105
PMIC primary	PMX35
PMIC clock	PMX35
38.4 MHz crystal	NDK EXS00A-CS12755
Power supply	
Single rail	3.8 V (typical) from the main board
Mechanical/thermal	
XY-dimension [mm]	28± 0.2 × 25.5± 0.2

Z-dimension [mm]	2.2 ± 0.2
PCB thickness [mm]	0.8 ± 10%
Mounting	Single side
Shielding	Two-piece metal shield 1.4 mm in height
Functional temperature [°C]	-30 to +75
Performance temperature [°C]	-20 to +60

2.2 Form factor

The following figure shows the AC5035 LGA module, which is manufactured on a 254-pin non-standard form factor.

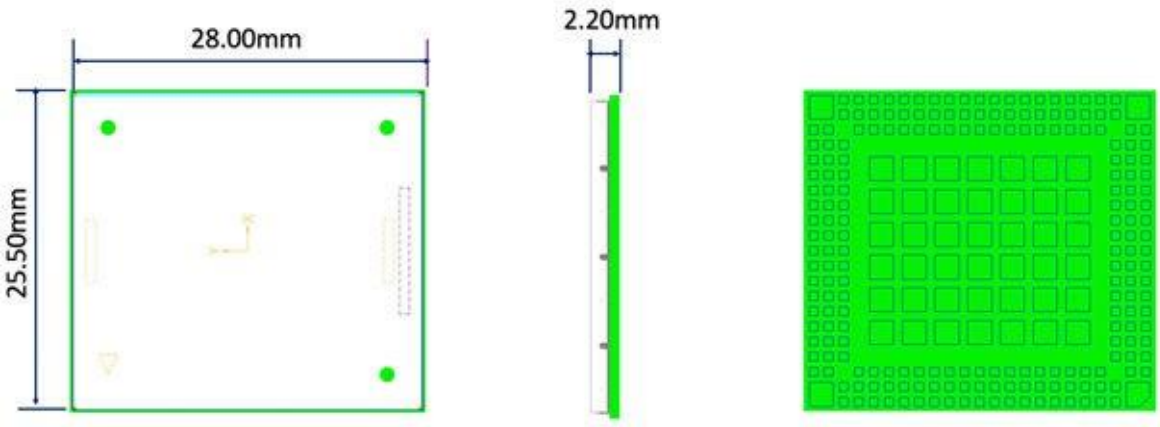

Figure 2-1 AC5035 LGA module form factor

For more information on the module's physical dimensions and connectors' locations please refer to chapter 6.

2.3 Pin Definitions

The SDX35 LGA pinout diagram is shown in the following figure.

Figure 2-2 AC5035 LGA pin diagram

2.4 I/O parameter definitions

Table 2-2 Pin attributes

Pin attribute	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
OD	Open drain

PU	Pull-up
PD	Pull-down

2.5 Pin descriptions

All the module pins are described in the following table.

NOTE More details will be updated in next revision

Table 2-3 Pin descriptions

Pin no.	Pin name	Pin characteristic		Module specific functional description
		Voltage	Type	
A1	AGND	–	–	Module ground
A3	SDC4_DATA2	1.8	PD:nppukp	Secure digital controller data2
A4	SDC4_DATA3	1.8	PD:nppukp	Secure digital controller data3
A5	SDC4_DATA1	1.8	PD:nppukp	Secure digital controller data1
A6	SDC4_DATA0	1.8	PD:nppukp	Secure digital controller data0
A7	SDC4_CLK	1.8	PD:nppukp	Secure digital controller clock
A8	SDC4_CMD	1.8	PD:nppukp	Secure digital controller 4 command
A9	AGND	–	–	Module ground
A10	HST_BT_UART_TX	1.8	PD:nppukp	UART_TX for WCN
A11	HST_BT_UART_CTS	1.8	PD:nppukp	UART_CTS for WCN
A12	AGND	–	–	Module ground
A13	NC	–	AO	PCIe Gen 2 transmit – plus
A14	NC	–	AO	PCIe Gen 2 transmit – minus
A15	NC	–	AI	PCIe Gen 2 receive – plus
A16	NC	–	AI	PCIe Gen 2 receive – minus
A17	NC	–	AO	PCIe Gen 2 reference clock – plus
A18	NC	–	AO	PCIe Gen 2 reference clock – minus
A19	AGND	–	–	Module ground
A20	SDX_DEBUG_UART_TX	1.8	PD:nppukp	System debug UART_TX

A21	SDX_DEBUG_UART_RX	1.8	PD:nppukp	System debug UART_RX
A23	AGND	–	–	Module ground
B3	AGND	–	–	Module ground
B4	PRI_MI2S_SCK	1.8	PD:nppukp	I^2S clock
B5	PRI_MI2S_WS	1.8	PD:nppukp	I^2S word select
B6	PRI_MI2S_DATA1	1.8	PD:nppukp	I^2S data1
B7	PRI_MI2S_DATA0	1.8	PD:nppukp	I^2S data0
B8	AGND	–	–	Module ground
B9	CODEC_INT1_N	1.8	PD:nppukp	CODEC interrupt
B10	HST_BT_UART_RX	1.8	PD:nppukp	UART_RX for WCN
B11	HST_BT_UART_RFR	1.8	PD:nppukp	UART_RFR for WCN
B12	NC	1.8	PU:nppukp	PCIe clock request
B13	AGND	–	–	Module ground
B14	SDX_SRST_N	1.8	DI	JTAG reset for debug
B15	AGND	–	–	Module ground
B16	SDX_TCK	1.8	DI	JTAG clock input
B17	AGND	–	–	Module ground
B18	SDX_GPIO_101	1.8	PD:nppukp	Configurable I/O
B19	AGND	–	–	Module ground
B20	SLEEPCLK_HST	–	DO	32 kHz sleep clock output for WCN
B21	FAULT_N	–	DI/DO	PMIC fault signal (bidirectional) that initiates shutdown or S3 reset.
C1	SDX_I2C_SCL	1.8	PD:nppukp	Platform I2C_SCL
C2	SDX_I2C_SDA	1.8	PD:nppukp	Platform I2C_SDA
C4	AGND	–	–	Module ground
C5	HST_SW_CTRL	1.8	PD:nppukp	WCN SW control
C6	WLAN_EN_1	1.8	PD:nppukp	WLAN enable
C7	AGND	–	–	Module ground
C8	MI2S_MCLK	1.8	PD:nppukp	MI2S_MCLK for WCD
C9	CODEC_RESET_N	1.8	PD:nppukp	WCD reset

C10	AGND	–	–	Module ground
C11	NC	1.8	PD:nppukp	PCIe reset
C12	NC	1.8	PU:nppukp	PCIe wake
C13	SDX_TRST_N	1.8	DI	JTAG reset
C14	SDX_TDO	1.8	Z	JTAG data output
C15	SDX_RESOUT_N	1.8	DO	Reset output
C16	SDX_TMS	1.8	B	JTAG mode select input
C17	SDX_TDI	1.8	DI	JTAG data input
C18	AGND	–	–	Module ground
C19	SDX_GPIO_75	1.2	PD:nppukp	Configurable I/O
C20	PMX_GPIO_08	–	MV	PMIC Configurable I/O
C22	AGND	–	–	Module ground
C23	RF_CLK2_WCN	–	DO	38.4 MHz RF XO clock buffer output 2
D1	AGND	–	–	Module ground
D2	BT_AUX_I2S_WS	1.8	PD:nppukp	I2S serial data word select for Bluetooth
D3	LE_BOOT_MODE	1.8	PD:nppukp	LE BOOT MODE key
D21	PMX_GPIO_05	–	MV	PMIC Configurable I/O
D22	AGND	–	–	Module ground
D23	VREG_DBB1_3P3_BB	3.3	PI	DBB 3.3V input for baseband
E1	BT_AUX_I2S_DATA0	1.8	PD:nppukp	I2S serial data channel 0 for Bluetooth
E2	BT_AUX_I2S_SCK	1.8	PD:nppukp	I2S clock for Bluetooth
E3	AGND	–	–	Module ground
E5	AGND	–	–	Module ground
E7	AGND	–	–	Module ground
E9	AGND	–	–	Module ground
E11	AGND	–	–	Module ground
E13	AGND	–	–	Module ground
E15	AGND	–	–	Module ground
E17	AGND	–	–	Module ground
E21	KPD_PWR_N	–	DI	Input pin generally connected to

				a keypad power-on button and when grounded, initiates the power-on sequence
E22	SDX_SLEEP_CLK1	–	DO	32 kHz sleep clock output for MDM
E23	VREG_S4A_1P8	1.824	PO	PMIC buck output
F1	BT_AUX_I2S_DATA1	1.8	PD:nppukp	I2S serial data channel 1 for Bluetooth
F2	VGI_SPI_MOSI	1.8	PD:nppukp	SLIC SPI MOSI
F3	PCIE_HOST_BYPASS	1.8	PD:nppukp	PCIe host bypass
F21	PMX_GPIO_04	–	LV	PMIC Configurable I/O
F22	VREG_S2A_1P22	1.224	PO	PMIC buck output
F23	VREG_S2A_1P22	1.224	PO	PMIC buck output
G1	VGI_SPI_CS_N	1.8	PD:nppukp	SLIC SPI CS
G2	AGND	–	–	Module ground
G3	SLIC_IRQ_N	1.8	PD:nppukp	SLIC IRQ
G5	AGND	–	–	Module ground
G7	AGND	–	–	Module ground
G9	AGND	–	–	Module ground
G11	AGND	–	–	Module ground
G13	AGND	–	–	Module ground
G15	AGND	–	–	Module ground
G17	AGND	–	–	Module ground
G21	PMX_GPIO_06	–	MV	PMIC Configurable I/O
G22	PMX_GPIO_02	–	LV	PMIC Configurable I/O
G23	PMX_GPIO_03	–	LV	PMIC Configurable I/O
H1	VGI_SPI_MISO	1.8	PD:nppukp	SLIC SPI MISO
H2	VGI_SPI_SCLK	1.8	PD:nppukp	SLIC SPI SCLK
H3	SLIC_RESET_N	1.8	PD:nppukp	SLIC reset
H21	AGND	–	–	Module ground
H22	AGND	–	–	Module ground
H23	AGND	–	–	Module ground
J1	AGND	–	–	Module ground

J2	EBI2_NAND_CS_N	1.8	PU:nppukp	EBI2_NAND_CS_N
J3	AGND	–	–	Module ground
J5	AGND	–	–	Module ground
J7	AGND	–	–	Module ground
J9	AGND	–	–	Module ground
J11	AGND	–	–	Module ground
J13	AGND	–	–	Module ground
J15	AGND	–	–	Module ground
J17	AGND	–	–	Module ground
J21	VPH_PWR	–	PI	Main input power
J22	VPH_PWR	–	PI	Main input power
J23	VPH_PWR	–	PI	Main input power
K1	EBI2_A_D6	1.8	PD:nppukp	EBI2_A_D6
K2	EBI2_A_D1	1.8	PD:nppukp	EBI2_A_D1
K3	EBI2_A_D4	1.8	PD:nppukp	EBI2_A_D4
K21	VPH_PWR	–	PI	Main input power
K22	VPH_PWR	–	PI	Main input power
K23	VPH_PWR	–	PI	Main input power
L1	EBI2_WE_N	1.8	PD:nppukp	EBI2_WE_N
L2	EBI2_A_D7	1.8	PD:nppukp	EBI2_A_D7
L3	EBI2_OE_N	1.8	PD:nppukp	EBI2_OE_N
L21	VREG_DBB1_3P3_RF	3.3	PI	DBB 3.3V input for RF
L22	AGND	–	–	Module ground
L23	AGND	–	–	Module ground
M1	EBI2_A_D5	1.8	PD:nppukp	EBI2_A_D5
M2	EBI2_CLE_UB_N	1.8	PD:nppukp	EBI2_CLE_UB_N
M3	EBI2_LCD_RESET_N	1.8	PD:nppukp	EBI2_LCD_RESET_N
M5	AGND	–	–	Module ground
M7	AGND	–	–	Module ground
M9	AGND	–	–	Module ground
M11	AGND	–	–	Module ground
M13	AGND	–	–	Module ground
M15	AGND	–	–	Module ground

M17	AGND	–	–	Module ground
M21	VREG_L6A_1P8	1.8	PO	PMIC LDO output
M22	AMBIENT_THERM	–	AI	AMUX input for quiet thermistor
M23	AGND	–		Module ground
N1	EBI2_A_D0	1.8	PD:nppukp	EBI2_A_D0
N2	EBI2_A_D3	1.8	PD:nppukp	EBI2_A_D3
N3	EBI2_LCD_A_D_8	1.8	PD:nppukp	EBI2_LCD_A_D_8
N21	VBUS_DET	–	DI	VBUS detect
N22	PS_HOLD	–	Z	Power-supply hold signal to PMIC
N23	ETH0_WOL_N	1.8	PD:nppukp	Ethernet WOL
P1	EBI2_A_D2	1.8	PD:nppukp	EBI2_A_D2
P2	EBI2_LCD_CS_N	1.8	PU:nppukp	EBI2_LCD_CS_N
P3	EBI2_LCD_TE	1.8	PD:nppukp	EBI2_LCD_TE
P5	AGND	–	–	Module ground
P7	AGND	–	–	Module ground
P9	AGND	–	–	Module ground
P11	AGND	–	–	Module ground
P13	AGND	–	–	Module ground
P15	AGND	–	–	Module ground
P17	AGND	–	–	Module ground
P21	ETH0_RESET_N	1.8	PD:nppukp	Ethernet reset
P22	AGND	–	–	Module ground
P23	AGND	–	–	Module ground
R1	AGND	–	–	Module ground
R2	AGND	–	–	Module ground
R3	AGND	–	–	Module ground
R21	EMAC_MDIO	1.8	PD:nppukp	EMAC management interface I/O
R22	SGMII_RX_M	–	–	SGMII interface serial data Rx – minus
R23	SGMII_RX_P	–	–	SGMII interface serial data Rx – plus

T1	AGND	–	–	Module ground
T2	SDX_GPIO_90	1.8	PD:nppukp	Configurable I/O
T3	AGND	–	–	Module ground
T5	AGND	–	–	Module ground
T7	AGND	–	–	Module ground
T9	AGND	–	–	Module ground
T11	AGND	–	–	Module ground
T13	AGND	–	–	Module ground
T15	AGND	–	–	Module ground
T17	AGND	–	–	Module ground
T21	SGMII_PHY_INTR_N	1.8	PD:nppukp	SGMII PHY interrupt
T22	SGMII_TX_M	–	–	SGMII interface serial data Tx – minus
T23	SGMII_TX_P	–	–	SGMII interface serial data Tx – plus
U1	AGND	–	–	Module ground
U2	FORCE_USB_BOOT	1.8	PD:nppukp	Forced USB boot 10K Ohm pull high to VREG_L6A_1P8 for USB Boot
U3	AGND	–	–	Module ground
U21	EMAC_MDC	1.8	PD:nppukp	EMAC management interface clock
U22	AGND	–	–	Module ground
U23	AGND	–	–	Module ground
V1	AGND	–	–	Module ground
V2	GNSS_ELNA_L1_EN	1.8	PD:nppukp	GNSS_ELNA_L1 enable (option, if no GPSS)
V3	GNSS_ELNA_L5_EN	1.8	PD:nppukp	GNSS_ELNA_L5 enable, (option, if no GPSS)
V21	PMX_GPIO_01	–	LV	PMIC Configurable I/O
V22	USB_HS_DP	–	AI/AO	USB high-speed data – plus
V23	USB_HS_DM	–	AI/AO	USB high-speed data – minus
W1	SDX_GPIO_92	1.8	PD:nppukp	Configurable I/O
W2	AGND	–	–	Module ground

W4	AGND	–	–	Module ground
W5	AGND	–	–	Module ground
W6	AGND	–	–	Module ground
W7	AGND	–	–	Module ground
W8	AGND	–	–	Module ground
W9	AGND	–	–	Module ground
W10	AGND	–	–	Module ground
W11	WLAN_TX_EN_TO_N79	1.8	DI	WLAN TX enable indicator IO
W12	AGND	–	–	Module ground
W13	SDX_RFFE6_CLK	1.8	PD:nppukp	RF front end interface clock
W14	SDX_GPIO_31	1.8	PD:nppukp	Configurable I/O
W15	AGND	–	–	Module ground
W16	UIM1_RESET	1.8/3	PD:nppukp	UIM1 reset
W17	FULL_CARD_PWR_OFF_RESIN_N	–	DI	Input pin used for generating a reset when held at a logic low
W18	UIM1_CLK	1.8/3	PD:nppukp	UIM1 clock
W19	AGND	–	–	Module ground
W20	UIM0_PRESENT	1.8/3	PD:nppukp	UIM0 presence detection
W22	VREG_L5A_1P8	1.8	PO	PMIC LDO output
W23	AGND	–	–	Module ground
Y3	AGND	–	–	Module ground
Y4	AGND	–	–	Module ground
Y5	AGND	–	–	Module ground
Y6	AGND	–	–	Module ground
Y7	AGND	–	–	Module ground
Y8	AGND	–	–	Module ground
Y9	AGND	–	–	Module ground
Y10	AGND	–	–	Module ground
Y11	AGND	–	–	Module ground
Y12	WLAN_COEX_SDX_UART_TX	1.8	PD:nppukp	UART_TX for WCN
Y13	SDX_RFFE6_DATA	1.8	PD:nppukp	RF front end interface data

Y14	SDX_GPIO_32	1.8	PD:nppukp	Configurable I/O
Y15	AGND	–	–	Module ground
Y16	ETH0_PWR_EN	1.8	PD:nppukp	Ethernet power enable
Y17	AGND	–	–	Module ground
Y18	n79_TX_EN_TO_WLAN	1.8	DO	N79 TX enable indicator IO
Y19	PMX_GPIO_07	–	MV	PMIC Configurable I/O
Y20	VREG_L15A_3P0	1.808	PO	PMIC LDO output
Y21	UIM1_PRESENT	1.8/3	PD:nppukp	UIM1 presence detection
AA1	AGND	–	–	Module ground
AA3	ANT1_CON	–	–	GNSS antenna (option)
AA4	AGND	–	–	Module ground
AA5	AGND	–	–	Module ground
AA6	ANT2_CON	–	–	RF DRX antenna
AA7	AGND	–	–	Module ground
AA8	ANT0_CON	–	–	RF TRX antenna
AA9	AGND	–	–	Module ground
AA10	AGND	–	–	Module ground
AA11	AGND	–	–	Module ground
AA12	WLAN_COEX_SDX_UART_RX	1.8	PD:nppukp	UART_RX for WCN
AA13	AGND	–	–	Module ground
AA14	UIM0_RESET	1.8/3	PD:nppukp	UIM0 reset
AA15	SDX_GPIO_76	1.2	PD:nppukp	Configurable I/O
AA16	UIM0_CLK	1.8/3	PD:nppukp	UIM0 clock
AA17	UIM0_DATA	1.8/3	PD:nppukp	UIM0 data
AA18	CBL_PWR_N	–	–	Cable power on
AA19	UIM1_DATA	1.8/3	PD:nppukp	UIM1 data
AA20	AGND	–	–	Module ground
AA21	VREG_L11A_3P0	1.808	PO	PMIC LDO output
AA23	AGND	–	–	Module ground

3. Electronics Specification

3.1 Absolute maximums

No functionality is guaranteed outside the following operating specifications.

Table 3-1 Absolute maximum ratings

Pin no.	Pin name	Parameter	Conditions	Min	Max	Unit
J21, J22, J23, K21, K22, K23	VPH_PWR	Supply voltage	–	3.3	4.4	V
		Ripple voltage	1 Hz to 100 KHz	–	100	mVpp

NOTE 1. Transmitter burst activity must also be accounted for in the 100 mVpp ripple limit.

2. To support input voltages lower than 3.3 V down to 3.135 V, a BoB converter must be added externally.

Further information will be provided in a future revision of this document.

4. Application interfaces

4.1 Universal serial bus (USB)

The legacy USB 2.0 is available in the module.

NOTE The table will be updated in a future release of the document.

Table 4-1 USB interface pins

Pin no.	Pin name	Pin Attribute	Functional description
V22	USB_HS_DP	DI/DO	High speed USB 2.0 data transmitter/receiver differential pair – positive
V23	USB_HS_DM	DI/DO	High speed USB 2.0 data transmitter/receiver differential pair – negative

4.2 User identity module (UIM)

Two UIM interfaces and one eSIM (optional) are available in the Module. In the default configuration, the UIM1 interface is connected to the eSIM (optional) while UIM0 is available for the use of an external SIM card. If the customer intends to have two external SIM cards, minor module rework will be required. The eSIM(optional) on LGA will have to be removed. Both UIM interfaces support Class B (3.0 V ± 10%) and Class C (1.8 V ± 10%) SIM cards.

Table 4-2 UIM0 and UIM1 interface pins

Pin no.	Pin Name	Pin Attribute	Functional description
AA14	UIM0_RESET	DO	SIM card 1 reset signal Active low
AA17	UIM0_DATA	DI/DO/PU	SIM card 1 bi-directional data signal
AA16	UIM0_CLK	DO	SIM card 1 reference clock signal
W20	UIM0_PRESENT	PU	SIM card 1 presence indication signal
W16	UIM1_RESET	DO	SIM card 2 reset signal Active low
AA19	UIM1_DATA	DI/DO/PU	SIM card 2 bi-directional data signal

W18	UIM1_CLK	DO	SIM card 2 reference clock signal
Y21	UIM1_PRESENT	PU	SIM card 2 presence indication signal

5. RF support

The following figure presents the RF high-level block diagram of the global LGA module, including its transceiver, antennas, low noise amplifiers (LNA), power amplifiers (PA), filters, and all its main connections.

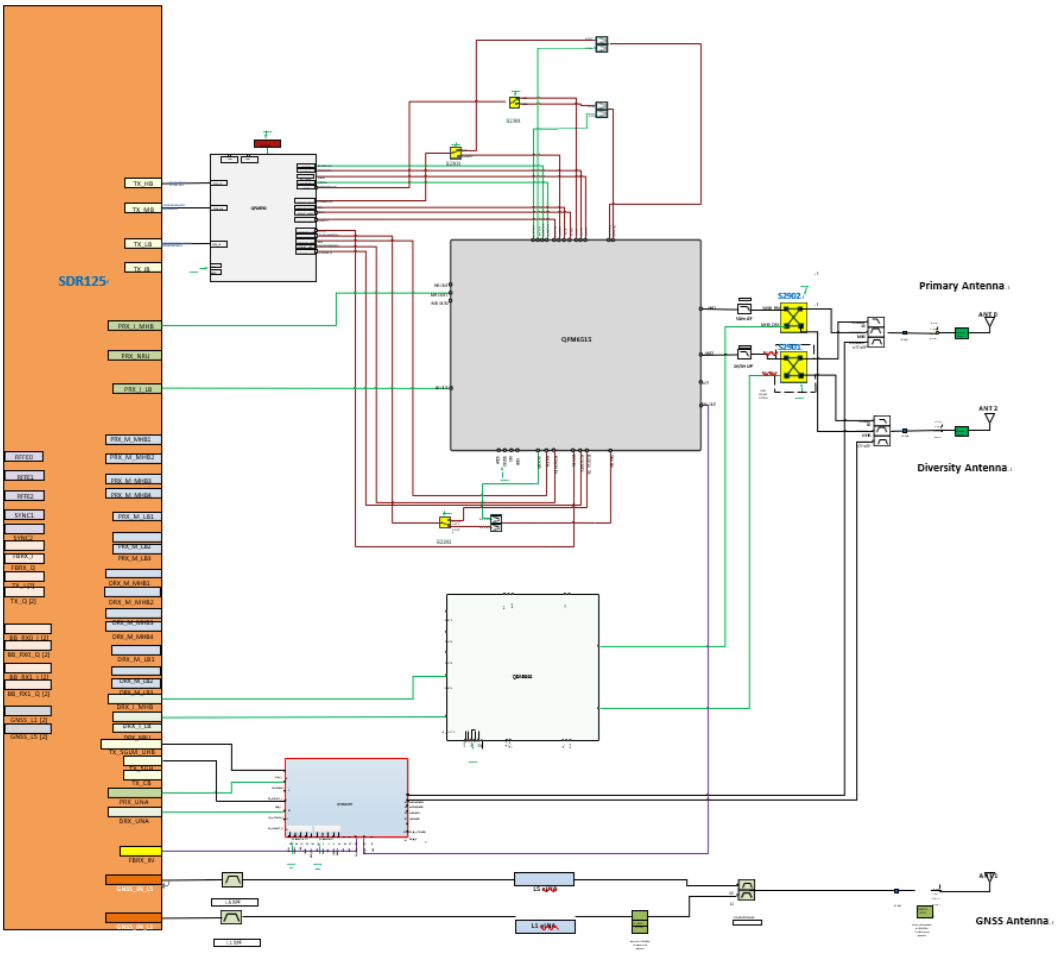

Figure 5-1 RF High-level block diagram

The frequency range of each antenna supported band group is listed in the following table.

Table 5-1 Antennas's band group frequencies

Port	Band group	Frequency range (MHz)
ANT0	LB TRX0	617–960
	MHB TRX0	1695–2690
	N77/N78/N79 TRX0	3300–5000
ANT2	LBRX1	617–960
	MHBRX1	1695–2690
	N77/N78/N79 RX1/SRS TX	3300–5000
ANT1 (option)	GNSS L1/L5	1164–1610

Following table lists the RF bands that the module supports on each technology.

Table 5-2 Supported RF bands

Technology	Supported bands
LTE	TDD: 34, 38, 39, 40, 41, 42, 43, 48 FDD: 1, 2/25, 3, 4/66, 5, 7, 8, 12, 13, 14, 17, 18, 19, 20, 26, 28, 30, 70, 71
Sub-6 5G NR	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30, n38, n40, n41, n48, n66, n70, n71, n77, n78, n79

6. Mechanical Information

The following figure provides a simplified high-level information on the device physical dimensions of AC5035 LGA module

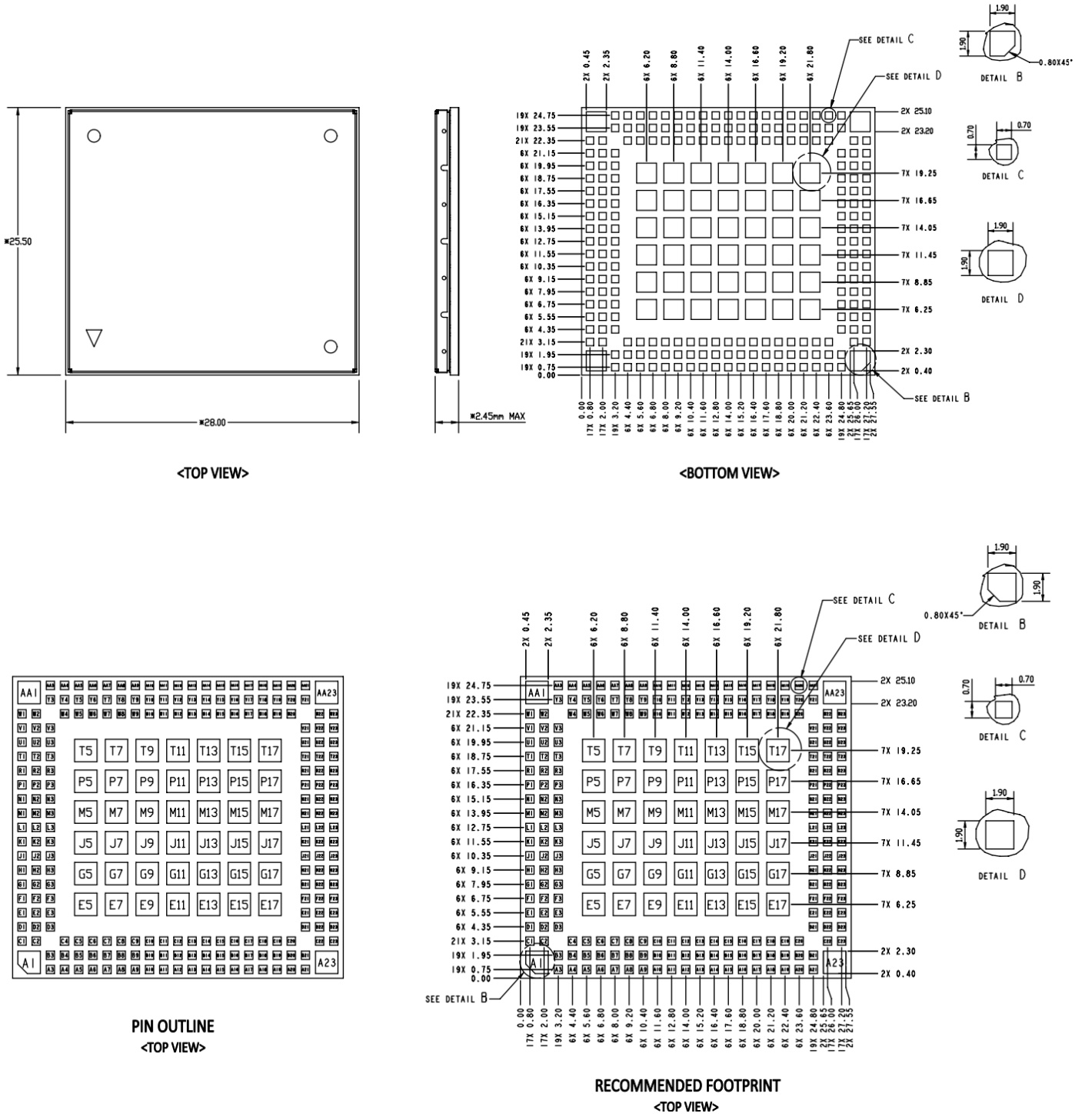

Figure 6-1 Module device physical dimension